IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) In a computer system having a scalar processing unit and a vector processing unit, wherein the vector processing unit includes a vector dispatch unit, a method of decoupling operation of the scalar processing unit from that of the vector processing unit, the method comprising:

sending a vector instruction from the scalar processing unit to the vector dispatch unit, wherein sending includes marking the vector instruction as complete if the vector instruction is not a vector memory instruction and if the vector instruction does not require scalar operands;

reading a scalar operand, wherein reading includes transferring the scalar operand from the scalar processing unit to the vector dispatch unit;

predispatching the vector instruction within the vector dispatch unit if the vector instruction is scalar committed;

dispatching the predispatched vector instruction if all required operands are ready; and

executing the dispatched vector instruction as a function of the scalar operand.

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2. (Previously Presented) The method according to claim 1, wherein executing the dispatched vector instruction includes translating an address associated with the vector instruction and trapping on a translation fault.

3. (Previously Presented) In a computer system having a scalar processing unit and a vector processing unit, wherein the vector processing unit includes a vector dispatch unit, a method of decoupling operation of the scalar processing unit from that of the vector processing unit, the method comprising:

sending a vector instruction from the scalar processing unit to the vector dispatch unit, wherein sending includes marking the vector instruction as complete if the vector instruction is not a vector memory instruction and if the vector instruction does not require scalar operands;